WHAT IS CLAIMED:

1. A system for simulating a circuit having both digital and analog components, wherein at least a portion of said circuit has been coded into a hardware description language (HDL) model, comprising:

a digital simulator that utilizes a programming language interface (PLI), wherein said digital simulator produces digital circuit information based on said HDL model;

an analog simulator that utilizes said PLI, wherein said analog simulator produces analog circuit information based on said HDL model; and

a mixed signal program that utilizes said PLI, that controls said digital and analog simulator, and that synchronizes a discrete digital time and a continuous analog time, wherein the use of said PLI by all three of said digital simulator, said analog simulator, and said mixed signal program comprises a mixed signal engine.

2. The system of claim 1, wherein said digital simulator includes an elaborator, wherein said elaborator converts a digital portion of a circuit net list description into an internal digital and instance structure database within said digital simulator, and wherein said analog simulator includes an elaborator, wherein said elaborator converts an analog portion of a circuit net list description into an internal database within said analog simulator.

3. The system of claim 2, wherein said mixed signal program operates to read the digital simulator database and transfer the digital simulator database to said analog simulator, wherein

said mixed signal program operates to read the analog simulator database and transfer the analog simulator database to said digital simulator, and wherein said mixed signal program utilizes the read data within the digital simulator database and the analog simulator database to perform a mixed signal interface processing function.

4. The system of claim 1, wherein said digital simulator includes an event engine to schedule a discrete time digital event.

5. The system of claim 1, wherein said analog simulator includes an analog circuit equation solver.

6. The system of claim 1, further comprising a time synchronizer that enables said mixed signal engine to schedule a PLI call back, wherein said PLI call back stops a digital simulation by said digital simulator so that said continuous analog time can advance to said discrete digital time or can move to a synchronization point.

7. The system of claim 1, further comprising a time synchronizer that enables said mixed signal engine to return from a PLI call back, wherein upon returning from said PLI call back, said digital simulator is advanced enabling said discrete digital time to advance to said continuous analog time or can move to a synchronization point.

8. The system of claim 1, further comprising a digital value changer that enables said mixed signal engine to schedule a value change call back on a digital signal, wherein upon a change in said digital signal said value change call back enable said mixed signal engine to change said digital signal to an analog value.

9. The system of claim 1, further comprising an analog to digital converter that enables said mixed signal engine to determine a digital value from an analog wave form pattern.

10. The system of claim 1, further comprising a digital to analog converter that enables said mixed signal engine to determine an analog value from a digital value.

11. The system of claim 1, wherein said digital simulator maintains a digital database and said analog simulator maintains an analog database, and wherein said mixed signal engine is able read a value from and write a value to said digital database and said analog database.

12. The system of claim 11, wherein the writing of said mixed signal engine to said digital database or said analog database provides for simulation control.

13. The system of claim 12, wherein said simulation control comprises a digital control script.

14. The system of claim 12, wherein said simulation control comprises an analog control script.

15. A method of analog mixed signal simulation for simulating a circuit, having both digital and analog components, that is described by one or more hardware description languages (HDLs), comprising the steps of:

reading the HDL;

elaborating the HDL for said digital components of said circuit;

elaborating the HDL for said analog components of said circuit;

performing a mixed signal elaboration on the HDL to determine digital and analog interaction locations;

performing a mixed signal initialization after said mixed signal elaboration; and

executing mixed signal simulation based on said mixed signal initialization wherein said step of executing includes digital simulation, analog simulation, and the synchronizing of a timing of said digital simulation with a timing of said analog simulation,

wherein each of the above steps are implemented at least in part by using a programming language interfaces (PLIs).

16. The method of claim 15, wherein said step of elaborating the HDL for said digital components comprises creating a digital circuit net list description and converting said digital net list description into a digital and instance structure database and wherein said step of elaborating

the HDL for said analog components comprises creating an analog circuit net list and converting said analog circuit net list into a database.

17. The method of claim 16, wherein said step of performing a mixed signal initialization includes reading the digital database and enabling said analog simulation to utilize data within said digital database, includes reading the analog database and enabling said digital simulation to utilize data within said analog database, and includes utilizing said data within said digital database and said analog database to perform mixed signal processing.

18. The method of claim 15, wherein said step of executing mixed signal simulation includes scheduling a discrete time digital event.

19. The method of claim 15, wherein said step of executing mixed signal simulation includes solving an analog circuit equation.

20. The method of claim 15, wherein said step of executing mixed signal simulation includes performing digital simulation.

21. The method of claim 15, wherein said step of executing mixed signal simulation includes scheduling a PLI call back, wherein said PLI call back stops a digital simulation enabling said timing of said analog component to advance to said timing of said digital component or to a pre-determined synchronization time.

22. The method of claim 15, wherein said step of executing mixed signal simulation includes returning from a PLI call back, wherein upon returning from said PLI call back, said timing of said digital component is advanced enabling said timing of said digital component to advance to said timing of said analog component or to a pre-determined synchronization time.

23. The method of claim 15, wherein said step of executing mixed signal simulation includes scheduling a value change call back based on a digital signal, wherein upon a change in said digital signal said value change call back enables the changing of said digital signal to an analog value.

24. The method of claim 15, wherein said step of executing mixed signal simulation includes determining a digital value from an analog wave form pattern.

25. The method of claim 15, wherein said step of executing mixed signal simulation includes determining an analog value from a digital value.

26. The method of claim 15, wherein said step of executing mixed signal simulation includes reading a value from and writing a value to a digital simulation database and an analog simulation database.

27. The method of claim 26, wherein writing a value to said digital simulation database or said analog simulation database provides for control of the execution of said mixed signal simulation.

28. The method of claim 27, wherein said value comprises a digital control script.

29. The method of claim 27, wherein said value comprises an analog control script.

30. A system for simulating a circuit having both digital and analog components, wherein at least a portion of said circuit has been coded into a hardware description language (HDL) model, said system comprising:

reading means for reading the HDL;

first elaborating means for elaborating the HDL for said digital components of said circuit;

second elaborating means for elaborating the HDL for said analog components of said circuit;

third elaborating means for performing a mixed signal elaboration on the HDL to determine digital and analog interaction locations;

initializing means for performing a mixed signal initialization after said mixed signal elaboration; and

executing means for executing mixed signal simulation based on said mixed signal initialization wherein said executing means includes a digital simulation means for

performing digital simulation, analog simulation means for performing analog simulation, and synchronizing means for synchronizing a timing of said digital simulation with a timing of said analog simulation,

wherein each of the above means utilizes a programming language interface (PLI).

31. The system of claim 30, wherein said first elaborating means includes means for creating a digital circuit net list description and means for converting said digital net list description into a digital and instance structure database. and wherein said second elaborating means includes means for creating an analog circuit net list and means for converting said analog circuit net list into a database.

32. The system of claim 31, wherein said initializing means includes means for reading the digital database and means for enabling said analog simulation means to utilize data within said digital database, includes means for reading the analog database and means for enabling said digital simulation means to utilize data within said analog database, and includes means for utilizing said data with said digital database and said analog database to perform mixed signal processing.

33. The system of claim 30. wherein said executing means includes a means for scheduling a discrete time digital event.

34. The system of claim 30, wherein said executing means includes a means for solving an analog circuit equation.

35. The system of claim 30, wherein said executing means includes a means for performing digital simulation.

36. The system of claim 30, wherein said executing means includes a means for scheduling a PLI call back, wherein said PLI call back stops a digital simulation enabling said timing of said analog simulation to advance to said timing of said digital simulation or to a pre-determined synchronization time.

37. The system of claim 30, wherein said executing means includes a means for returning from a PLI call back, wherein upon returning from said PLI call back, said timing of said digital simulation is advanced enabling said timing of said digital simulation to advance to said timing of said analog simulation or to a pre-determined synchronization time.

38. The system of claim 30, wherein said executing means includes means for scheduling a value change call back based on a digital signal, wherein upon a change in said digital signal said value change call back enables the changing of said digital signal to an analog value.

39. The system of claim 30, wherein said executing means includes a means for determining a digital value from an analog wave form pattern.

40. The system of claim 30, wherein said executing means includes a means for determining an analog value from a digital value.

41. The system of claim 30, wherein said executing means includes a means for reading a value from digital simulation database or an analog simulation database, and a means for writing to a digital simulation database or an analog simulation database.

42. The system of claim 41, wherein writing a value to said digital simulation database or said analog simulation database provides execution control for said execution means.

43. The system of claim 42, wherein said value comprises a digital control script.

44. The system of claim 42, wherein said value comprises an analog control script.